REMARKS

Prior to examination on the merits, please amend the specification as indicated in attached Appendix A, and please cancel claim 1 (claims 2-49, 63-84, and 94-96 have been canceled in the transmittal document accompanying this preliminary amendment) without prejudice, amend claims 50, 54, and 89, and add claims 97 and 98 as indicated in attached Appendix B. Claims 50-62, 85-93, 97, and 98 should now be pending in the present application.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX A

~~CO-PENDING~~ CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application is a divisional of U.S. Patent Application No. 09/839,642, filed on April 20, 2001, entitled "Multiple Channel Modules And Bus Systems Using Same", which ~~This~~ is a continuation-in-part of U.~~nited~~ S.~~tates~~ Patent Application No. 09/568,424, filed May 10, 2000, both of which are hereby incorporated by reference herein in their entirety.

APPENDIX B

1-49 (Canceled).

50 (Currently Amended). A module having first and second primary surfaces and having a first end, the module comprising:

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first terminator disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a first bus including a first channel extending from the first set of input finger connectors to the first terminator, the first bus connected to a first IC of the plurality of ICs; and

a second bus including a second channel extending from the second ~~IC~~ set of input finger connectors to the second terminator, the second bus connected to a second IC of the plurality of ICs.

51 (Original). The module of claim 50 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

52 (Original). The module of claim 50 wherein the first IC of the plurality of ICs and the second IC of the plurality of ICs are mutually exclusive.

53 (Original). The module of claim 50 wherein the first channel and the second channel allow simultaneous independent access to the plurality of ICs.

54 (Currently Amended). The module of claim 50 further comprising:

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a third terminator disposed on at least one of the first and second primary surfaces;

a fourth terminator disposed on at least one of the first and second primary surfaces; ~~and~~

a third bus including a third channel extending from the third set of input finger connectors to the third terminator; and

a fourth bus including a fourth channel extending from the fourth set of input finger connectors to the fourth terminator.

55 (Original). The module of claim 54 wherein the third bus is connected to a third IC of the plurality of ICs and wherein the fourth bus is connected to a fourth IC of the plurality of ICs.

56 (Original). The module of claim 55 wherein the first IC of the plurality of ICs, the second IC of the plurality of ICs, the third IC of the plurality of ICs, and the fourth IC of the plurality of ICs are mutually exclusive.

57 (Original). The module of claim 54 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

58 (Original). The module of claim 54 wherein the first set of input finger connectors and the second set of input finger

connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input finger connectors are disposed on the second primary surface.

59 (Original). The module of claim 54 wherein the first channel, the second channel, the third channel, and the fourth channel each allow simultaneous independent access to the plurality of ICs.

60 (Original). The module of claim 50 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, each of the paths being coupled to at least one of the plurality of ICs, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

61 (Original). The module of claim 50 wherein the first bus is connected to a first set of the plurality of ICs, the first set comprising the first IC, and the second bus is connected to a second set of the plurality of ICs, the second set comprising the second IC.

62 (Original). The module of claim 61, wherein each of the ICs

are memory devices.

63-84 (Canceled).

85 (Original). A module having first and second primary surfaces and having a first end, the module comprising:

a first integrated circuit (IC) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first set of output finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a terminator disposed on at least one of the first and second primary surfaces;

a first bus including a first channel extending from the first set of input finger connectors to the first set of output finger connectors, the first bus connected to the first IC; and

a second bus including a second channel extending from the second set of input finger connectors to the terminator.

86 (Original). The module of claim 85 further comprising:

a second IC, wherein the second bus is coupled to the second IC.

87 (Original). The module of claim 86 wherein the first channel and the second channel allow simultaneous independent access to the first IC and the second IC.

88 (Original). The module of claim 85 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

89 (Currently Amended). The module of claim 8~~5~~6 further comprising:

a third integrated circuit (IC) populating at least one of the first and second primary surfaces;

a fourth integrated circuit (IC) populating at least one of the first and second primary surfaces;

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of output finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a third bus including a third channel extending from the third set of input finger connectors to the second set of output finger connectors, the third bus connected to the third IC; and

a fourth bus including a fourth channel extending from the fourth set of input finger connectors to the second terminator.

90 (Original). The module of claim 89 wherein the first channel, the second channel, the third channel, and the fourth channel allow simultaneous independent access to the first IC, the second IC, the third IC, and the fourth IC.

91 (Original). The module of claim 89 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

92 (Original). The module of claim 89 wherein the first set of input finger connectors and the second set of input finger connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input

finger connectors are disposed on the second primary surface.

93 (Original). The module of claim 85 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

94-96 (canceled).

97 (New). A module having first and second primary surfaces and having a first end, the module comprising:

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces;

first input connector means disposed on at least one of the first and second primary surfaces;

second input connector means disposed on at least one of the first and second primary surfaces;

first terminator means disposed on at least one of the first and second primary surfaces;

second terminator means disposed on at least one of the first and second primary surfaces;

first bus means including a first channel extending from

the first input connector means to the first terminator means, the first bus means connected to a first IC of the plurality of ICs; and

second bus means including a second channel extending from the second input connector means to the second terminator means, the second bus means connected to a second IC of the plurality of ICs.

98 (New). A module having first and second primary surfaces and having a first end, the module comprising:

a first integrated circuit (IC) populating at least one of the first and second primary surfaces;

first input connector means disposed on at least one of the first and second primary surfaces;

first output connector means disposed on at least one of the first and second primary surfaces;

second input connector means disposed on at least one of the first and second primary surfaces;

terminator means disposed on at least one of the first and second primary surfaces;

first bus means including a first channel extending from the first input connector means to the first output connector means, the first bus means connected to the first IC; and

second bus means including a second channel extending from the second input connector means to the terminator means.